IN THE CLAIMS

1.   (Currently Amended)   A logic circuit comprising:

a control flow logic to select a trace descriptor for processing including at least one dependency descriptor, the dependency descriptor including dependency information for ~~each~~ an instruction sequence and a location of the instruction sequence; and

a data flow logic coupled to the control flow logic to execute the ~~a plurality of~~ instruction sequence~~s~~ according to the dependency information stored in the dependency descriptor.

2.   (Currently Amended)   The logic circuit of claim 1 further comprising a first storage area coupled to the control flow logic and the data flow logic, the first storage area to store the dependency descriptor after separation from a selected trace descriptor by the control flow logic.

3.   (Currently Amended)   The logic circuit of claim 2 further comprising a second storage area coupled to the control flow logic, the second storage area dedicated to ~~store~~ storage of ~~a~~ trace descriptor~~s~~.

4.   (Original)   The logic circuit of claim 3 further comprising a third storage area coupled to the data flow logic, the third storage area to store instructions contiguously based on dependency information.

5.   (Original)   The logic circuit of claim 4 further comprising a fourth storage area coupled to the data flow logic and control flow logic, the fourth storage area to store live-out data.

6.   (Original)   The logic circuit of claim 5 further comprising a fifth storage area coupled to the control flow logic, the fifth storage area to map live-in and live-out data.

7.   (Original)   The logic circuit of claim 6 wherein each of the storage areas are in at least one memory device.

8.   (Currently Amended)   The logic circuit of claim 1 wherein the trace descriptor includes aggregate live-in data for ~~the at least one~~ a plurality of dependency descriptors in the trace description.

9.   (Currently Amended)   The logic circuit of claim 1 wherein the trace descriptor includes aggregate live-out data for ~~the at least one~~ a plurality of dependency descriptor in the trace description.

10.   (Currently Amended)   A computer system comprising:
at least one memory device;
a bus coupled to the at least one memory device;
a control flow logic device to analyze dependencies among instruction sequences in a trace and ~~creates~~ a trace descriptor comprising a dependency descriptor ~~including~~ indicating a live-in value ~~dependency information~~ for ~~each~~ an instruction sequence; and
a data flow logic device coupled to the control flow logic to execute a plurality of the instruction sequences according to the dependency information stored in the dependency descriptor.

11.   (Currently Amended)   The computer system of claim 10 further comprising ~~a first storage area~~ a dependency claim issue window coupled ~~to~~ between the control flow logic device and the data flow logic device, the ~~first storage area~~ dependency data issue window to store the dependency descriptor.

12.   (Currently Amended)   The computer system of claim 11 further comprising a second storage area coupled to the control flow logic_device, the second storage area to store a trace descriptor.

13.   (Currently Amended)   The computer system of claim 12 further comprising a third storage area coupled to the data flow logic_device, the third storage area to store instructions contiguously based on dependency information.

14.   (Currently Amended)   The computer system of claim 13 further comprising a fourth storage area coupled to the data flow logic_device and control flow logic_device, the fourth storage area to store-live-out data.

15.   (Original)   The computer system of claim 14 further comprising a fifth storage area coupled to the control flow logic, the fifth storage area to map live-in and live-out data.

16.   (Original)   The computer system of claim 15 wherein each of the storage areas are in at least one memory device.

17.   (Currently Amended)   The computer system of claim 10 wherein the trace descriptor includes aggregate live-in data for the at least onea plurality of dependency descriptors in the trace description.

18.   (Currently Amended)   The computer system of claim 10 wherein the trace descriptor includes aggregate live-out data for the at least onea plurality of dependency descriptors in the trace description.

19.   (Currently Amended)   The computer system of claim 10 wherein the dependency descriptor includes live-in and a live-out data-value for the dependency informationinstruction sequence.

20.   (Currently Amended)   A method of processing instructions comprising:

fetching a trace descriptor;

separating out a dependency descriptor including dependency information for a set of instructions from the trace descriptor;

fetching the set of instructions ~~described~~ at a location indicated by the dependency descriptor; and

executing a plurality of the instruction sequences according to ~~the~~ dependencies stored in the dependency descriptor.

21.   (Original)   A method according to claim 20 further comprising:

updating live-out data in a first storage area.

22.   (Currently Amended)   A method according to claim 21 further comprising:

storing the dependency descriptor extracted by ~~the~~ a control flow logic into a second storage area; and

reading the descriptor out of the second storage area into ~~the~~ a data flow logic.

23.   (Original)   A method according to claim 22 wherein the fetching of a set of instructions is completed just in time for execution.

24.   (Original)   A method according to claim 23 wherein the instructions are out of order.

25.   (Original)   A method according to claim 24 further comprising:

updating the architectural state using the data in the first storage area.

26.   (Original)   A method according to claim 25 further comprising:

recovering an earlier architectural state after a misprediction using the data in the first storage area.

27.   (Currently Amended)   A method according to claim 20 further wherein ~~the~~ selecting involves predicting the next trace descriptor to process.

28.   (Currently Amended)   A machine-readable medium that provides instructions, which when executed by a machine cause the machine to perform operations comprising:

fetching a trace descriptor;

separating out a dependency descriptor including dependency information for a set of instructions from the trace descriptor;

___storing the dependency descriptor in an issue window to await assignment to an execution unit;___

fetching the set of instructions described by_the dependency descriptor; and

executing ~~a plurality~~the set of the instruction~~s~~ ~~sequences~~according to the dependencies stored in the dependency descriptor.

29.   (Original)   The machine-readable medium of Claim 28, wherein the operations further comprise:

updating live-out data in a first storage area.

30.   (Currently Amended)   The machine-readable medium of Claim 29, wherein the operation further comprise:

~~storing the dependency descriptor extracted by the control flow logic into a second storage area; and~~

reading the descriptor out of the ~~second storage area~~issue window into the data flow logic.